Remarks/Arguments

Summary

Claims 1, 8, and 15 have been amended. Claims 1, 2, 4-9, 11-16, and 18-25 remain pending in this application.

Improper Finality of Rejection

In the office action dated July 31, 2006, claims 1-2, 4-9, 11-16, and 18-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,466,496 to Kuge et al. (hereafter, "Kuge") in view of U.S. Patent No. 6,233,650 to Johnson et al. (hereafter, "Johnson"). The rejection was improperly made final because the rejection was based on newly cited art (Johnson) and at least one claim was not amended to require the newly cited art. For example, independent claim 8 was not amended in response to the previous office action. Moreover, the office action admits that the applicants' arguments submitted on 5/18/06 in response to the previous office action were "fully considered and are persuasive." (See, Office Action, section 4). Thus, the rejection of the unamended claims plainly constitutes a new ground of rejection, and thus should not have been made final.

According to the MPEP, "a second or any subsequent action on the merits in any application or patent undergoing reexamination proceedings will not be made final if it includes ***a rejection, on newly cited art***, other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17 (p), of ***any claim not amended by applicant*** or patent owner in spite of the fact that other claims may have been amended to require newly cited art." (See, MPEP 706.07(a), emphasis added).

Since the finality of the current office action is a violation of the applicants' right to fair prosecution under current office practice, the applicants respectfully request that the finality of the office action be withdrawn.

Because the finality of the rejection was improper, applicants have amended the claims and request entry of the amendments as a matter of right.

Telephone Conversations – October 17-18, 2006

A request for a personal face-to-face interview was denied in a telephone conversation with Examiner Phan on October 17, 2006. However, various features of claim 1 were discussed in later telephone conversations with the examiner on October 17 and 18. In the conversations, the examiner agreed that an amendment could be used to overcome the rejections to the claims.

Claim Rejections - 35 U.S.C. § 103(a)

Claims 1-2, 4-9, 11-16, and 18-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuge in view of Johnson. These rejections have been obviated by amendments to the claims, in which language was added to clarify the definition of certain features. Although certain claims have been amended, the following explanation is nevertheless provided to demonstrate several ways in which the claims define over Kuge and Johnson.

The office action begins by stating that Kuge discloses "system data buses DQ each having a multi-bit structure (see lines 47, column 5) which may be a 32-bit (see lines 60, column 7), therefore, each system data bus must inherently have a width of M bits, where M can be a natural number or 32." (See, Office Action, section 2). Whether or not this statement is even true, it fails to address any specifically recited element of any of the claims. For example, independent claims 1, 8, and 15 define "N system data buses having a width of M/N bits" – not simply a bus with a width of M bits. Absent a showing that Kuge discloses N system data buses, each with a width or M/N, the rejection of independent claims 1, 8, and 15 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

The office action continues by stating that Kuge discloses in FIG. 3 a plurality of memory module groups "group 1 (1000A and 1000B), group 2 (1000B and 1000C)". In other words, the office action maintains that Kuge discloses first through P-th memory module groups, each having N memory modules, wherein P=2 and N=2.

The office action then states that "the length of data transmission line/data transmission time can be made equal in compliance with JEDEC standard through line folding (see lines 23-29, column 3 and lines 66-67, column 5) which is read on the

feature 'wherein the N system data buses are wired such that data transmission times between the N memory modules within each of the first through P-th module groups and the memory controller are the same'". (See, office action, section 2). The office action's conclusion in the above statement is without merit.

Contrary to the office action's interpretation, the actual meaning of the cited text at column 3, lines 23-29, is that the lengths of various data transmission lines from the system controller in Kuge and selected endpoints are the same as *each other*. The text does not suggest that the data transmission lines have the same length to each of the endpoints. For example, as illustrated in FIG. 1 of Kuge, data transmission lines 2a~2m each have the same length as *each other* between system controller 1 and memory module 1000A. Data transmission lines 2a~2m also have the same length as *each other* between system controller 1 and memory module 1000B. However, the length of data transmission lines 2a~2m between system controller 1 and memory module 1000A is less than the length of data transmission lines 2a~2m between system controller 1 and memory module 1000B.

Contrary to the office action's erroneous interpretation, Kuge explains its reference to the JEDEC standard by stating "In DDR-SDRAMs, a data transmission line for data transmission, a signal line for transmission of a data strobe signal DQS and a signal line for transmission of a clock signal are required to be of the same length [*as each other!*] based on the JEDEC standard." (See, Kuge at column 5, lines 51-58). Further, the figures in Kuge clearly show that the respective lengths of the data transmission lines between system controller 1 and memory modules 1000A, 1000B, and 1000C are *not* the same. For example, FIG. 4 of Kuge provides another view of the system shown in FIG. 3, wherein a data transmission line 2 passes through a node "na" connected to memory module 1000A before reaching a node "nb" similarly connected to memory module 1000B. Since all of the figures in Kuge actually illustrate that the respective lengths of the data transmission lines between system controller 1 and memory modules 1000A, 1000B, and 1000C are *different*, and since Kuge provides no disclosure to the contrary, the office action's suggestion that Kuge discloses data transmission lines having the same length / transmission times between system

controller 1 and each of memory modules 1000A, 1000B, and 1000C is completely unfounded.

Since Kuge never discloses "N system data buses...wired such that data transmission times between the N memory modules within each of the first through P-th module groups and the memory controller are the same," the rejection of independent claims 1, 8, and 15 is unwarranted and should be withdrawn.

As further evidence that the data transmission times (and lengths) between system controller 1 and memory modules 1000A, 1000B, and 1000C are *not* the same, Kuge describes that the data transmission distance between system controller 1 and each memory module is *independently* tested using a test circuit so that a setup and hold time can be individually established for transmission between system controller 1 and each of memory modules 1000A through 1000C. In other words, Kuge treats the data transmission times (and lengths) between system controller 1 and memory modules 1000A through 1000C as different its specification because they *are* different.

Because Kuge never discloses "N system data buses...wired such that data transmission times between the N memory modules within each of the first through P-th module groups and the memory controller are the same," the rejection of independent claims 1, 8, and 15 is improper and should be withdrawn. For at least this and other reasons described above, the rejection of associated dependent claims 2, 4-7, 9, 11-14, 16, and 18-25 is also improper and should be withdrawn.

The office action also states that Kuge discloses "memory banks B0-B7," apparently asserting that these banks read on claims 4-5, 11-12, and 18-19. However, as explained in response to the previous office action dated February 27, 2006, the office action fails to identify "L devices" in each bank, or appropriate data bus widths such as those defined, for example, in claims 4, 6, 11, 13, 18, or 20. Kuge simply teaches that all of banks B0-B7 are connected to a common data input/output bus G-I/O with an unspecified bit width. (See, Kuge at Fig. 8). In other words, Kuge fails to disclose most, if not all of the technical content of claims 4-5, 11-12, and 18-19 regarding bus widths, number of devices, and so on. Since Kuge fails to disclose each element of claims 4-5, 11-12, and 18-19, Kuge does not support a rejection of these claims under 35 U.S.C. § 103(a).

The office action later states that Kuge does not disclose that the so-called memory module groups made up of memory modules 1000A and 1000B, and memory modules 1000B and 1000C, respectively, are "operated in response to respective first through P-th chip select signals as recited in claims 1, 8, and 15." (See, office action, section 2). The office action then claims that it would have been obvious to combine the teachings of Johnson, which discloses providing one chip select signal to multiple chips, with the system of FIG. 3 in Kuge so that a first chip select signal is used to control memory modules 1000A and 1000B and a second chip select signal is used to control memory modules 1000B and 1000C. The office action's reasoning is flawed on several counts.

For example, first, according to the office action's suggestion, memory module 1000B would be controlled in response to both the first and second chip select signals. One of ordinary skill in the art would not be motivated to control memory module 1000B with both chip select signals because it creates an unnecessary control hazard and introduces unnecessary complexity into the memory architecture; thus, it doesn't seem to make much technical sense.

Further, one skilled in the art would not be motivated to control two of the memory modules in FIG. 3 of Kuge with the same chip select signal because, according to the disclosure of Kuge, the timing of each of memory modules 1000A, 1000B, and 1000C is intended to be independent. (See, e.g., Kuge at col. 3, lines 13-15). For example, memory modules 1000A, 1000B, and 1000C have unique, different hold and set up times and data transmission times. Accordingly, one skilled in the art would not be motivated to control these memory modules with the same chip select signal.

Since there is no motivation to combine the teachings of Kuge and Johnson, the rejection of independent claims 1, 8, and 15, together with their associated dependent claims under 35 U.S.C. § 103(a) is unjustified and should be withdrawn.

In conclusion, the Office Action rejected claims 1-2, 4-9, 11-16, and 18-25 under 35 U.S.C. § 103(a) as being unpatentable over Kuge in view of Johnson without showing disclosure in Kuge or Johnson related to several claimed elements, and without demonstrating any motivation to combine the teachings of Johnson with Kuge. In addition, the rejection was improperly made final because the rejection relied on

newly cited art to reject unamended claims. Accordingly, removal of the finality of this rejection and reconsideration and a favorable action on claims 1-2, 11-16, and 18-25 is respectfully requested.

Respectfully submitted,

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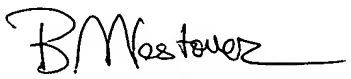

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